A Highly Integrated MMIC Chipset for 60 GHz Broadband Wireless Applications

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Abstract — **A full and flexible MMIC (monolithic microwave integrated circuit) chipset has been developed for 60 GHz broadband wireless applications. It is based on several circuits operating in the 55-65 GHz frequency range. The MMICs have been fabricated on UMS commercially available 0.25 and 0.15 µm GaAs pHEMT processes. This chipset is focused on a MMIC multifunction chip (MFC) including a sub-harmonic mixer and a LO buffer allowing carrier 2xLO suppression and image rejection. Several frequency multipliers by 2, 3 and 4 have been produced for the LO supply chain and use balancing topologies leading to fundamental or even-harmonics suppression improvement. Finally, a complete family of low noise/medium power amplifiers is described in this paper. All the circuits have been designed in order to ease the integration, to reduce the size and finally to reach the cost requirements for such systems.**

I. Introduction

The development of interactive multimedia services (telephone, video, computer datas) and fast Internet access requires higher and higher speed and capacity. Broadband Wireless systems at millimeter wave frequencies offer an interesting, fast and cost effective solution for indoor and outdoor professional and consumer applications like Point-to-Point, Point-to-Multi-Point, WLAN.

The 60 GHz frequency range is particularly well suited for short distance in high density area, thanks to the additional oxygen absorption around this frequency. This characteristic reduces the interferences between nearby transmitters and allows a higher density.

Based on customers recommendations and following similar work in other frequency ranges like LMDS @ 28 GHz [1] and MVDS @ 42 GHz [2], the first pass of a full V-band MMIC chipset has been developed. Compared to previous publications [3] [4] [5], the frequency range has been extended to 55-65 GHz in order to be compliant with systems proposed in United States, Japan and Europe.

In this paper, we present the performances of this MMIC chipset, which involves innovative topologies and techniques, leading to excellent performances, reduced sizes, high integration, high transceiver architecture flexibility and finally reduction of the overall cost of the radio transceiver.

II. General Architecture Description

A. Transceiver Topology Example

A typical 60 GHz transceiver frontend block diagram is shown in figure 1. This example is not exhaustive and may change to meet system requirements.

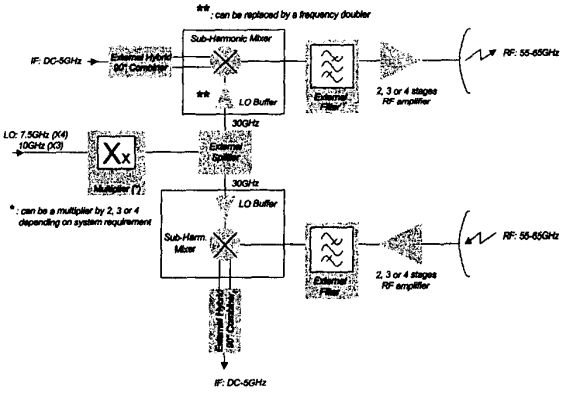

Fig. 1. Example of a transceiver block diagram.

The chipset presented in this paper has the strong advantage to be very adaptable to the customers' requirements.

Firstly, a full family of frequency multipliers has been developed for the LO chain, allowing the customers to choose the appropriate multiplication factor according to their LO signal generation constraints (e.g: VCO phase noise).

Secondly, the mixer has been designed in order to ease the external filter design by allowing internal carrier

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2xLO suppression and image rejection; the same chip can also be used in both transmit and receive paths with extended IF frequency range.

Finally, two new low noise amplifiers have been added to the 2 stages amplifier CHA2157 to give to customers the opportunity to find the right gain level / noise figure combination in their module design; these RF amplifiers are also designed for power functionality and can be used as transmit final stages before the antenna.

B. MMICs technologies

All the MMICs reported have been fabricated on UMS commercial GaAs pseudomorphic pHEMT 0.25 and 0.15 µm processes. These are fully available in production and are dedicated to very low-noise and small/medium power circuits. Their typical f_T are 90 GHz and 110 GHz respectively. These processes include via holes, compound semiconductor and metallic resistances and MIM capacitors. The substrate thickness is 100 µm.

In the frame of the development of the 55-65 GHz chipset, a new technological step has been evaluated. This step consists in the deposition of a surface passivation layer over the whole chip surface, except areas where it is mandatory to connect bonding wires (i.e: in/out RF cells, DC pads). Thanks to this new layer, the chips are completely protected against humidity and all other external pollution.

For this first pass, the passivation layer has not been taken into account during simulation but, despite the modification of the electromagnetic environment, measurements exhibit minor discrepancy. Nevertheless, the influence of the surface passivation layer can be easily taken into account and compensated during simulation, thanks to electromagnetic simulators, and can be considered finally transparent from the electrical performances point of view.

Due to the fact that the module does not require anymore hermeticity, this protection relaxes the module design's constraints, and leads to reduction of the global transceiver cost.

III. Circuits Description & Measured Performances

A. Multifunction mixer

This MMIC integrates a 25-35 GHz LO buffer amplifier and a single side band mixer (IRM and 2xLO suppression). The sub-harmonic approach was chosen in order to reduce the required chip size. It suppresses the need for a multiplier on the LO side, and allows to design a Single Side Band (SSB) mixer with half the size compared to a fundamental mixer, thanks to the anti-parallel topology of the diodes. This particular topology naturally suppresses the second harmonic of the LO signal at the output of the mixer. So, to realize a SSB mixer, we only need two individual mixing cells balanced in quadrature, thanks to an integrated Lange coupler and an external hybrid 90° combiner. Furthermore, this topology is usable for both up and down conversion.

The mixer has been designed for IF working up to 5 GHz. The typical DC polarization is Vdd = 3.5 V and Idd = 90 mA. The chip size is 2.3 mm².

The layout of this MMIC is displayed on figure 5.

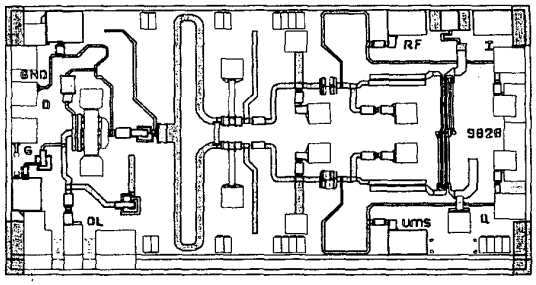

Fig. 5. Layout of the multifunction MFC mixer.

The on-wafer measurements exhibit conversion losses better than 12 dB with IF=2.0GHz. The image rejection is better than –10dB and the 2xLO leakage is –36 dBm (for input LO power equal to +10 dBm). The 1dB input compression point is higher than 0 dBm at RF=62GHz – LO=30GHz.

All these results are resumed by the figure 6.

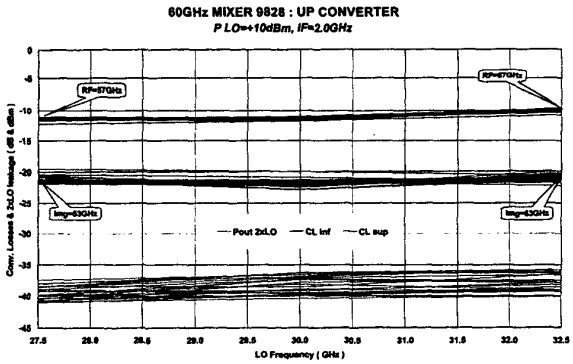

Fig. 6. Conversion Losses, Image Rejection and 2xLO Leakage versus LO Frequency (LO power = +10 dBm – IF = 2.0 GHz).

B. Low Noise / Medium Power Amplifiers

Two different LNA have been developed in order to fulfill the customers requirements in term of gain and noise. Precisely, they are 3 stages and 4 stages, leading to

15 dB and 20 dB gain on the frequency range 55-65 GHz respectively. Their noise figures are lower than 4.0 dB. Their respective sizes are 2.1 and 2.6 mm². Their DC consumption are 90 mA and 115 mA respectively under 3.5V. The last stage has been designed also for power functionality, so that the MMICs can be placed as final transmit amplifier. Their typical P_{1dB} value is about +15 dBm.

They complete the UMS CHA2157, which is a 2 stage amplifier (10 dB gain, 4.0 dB noise figure and 15 dBm P_{1dB} – 1.8 mm²).

The figure 10 gives the typical on-wafer S-parameters and noise figure measurements of this chip.

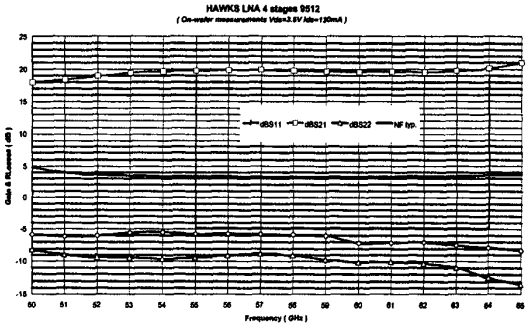

Fig. 10. Typical On-wafer S-parameters and Noise Figure of the 4 stages amplifier.

C. Transmitter Frequency Doubler X2

In some circumstances, due to system design, the information can be transmitted directly through the LO signal. In that case, the Up-Converter can be replaced by a frequency multiplier by 2 (X2) from 30 to 60 GHz.

The topology is based on a first stage working as the multiplier which is supplied by a balun coupler. It is followed by a 55-65 GHz 2 stages buffer.

The innovative balun topology improves the fundamental rejection on the output by splitting the input signal with opposite phases and combining them on multiplier's output through a simple in-phase combiner.

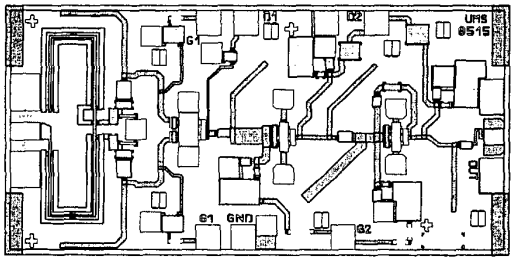

Fig. 11. Layout of the frequency multiplier by 2 (X2) 30→60 GHz.

The layout of this MMIC is shown on figure 11. The chip size is 2.35 mm² and the typical DC consumption is 70 mA at 3.5 V.

The typical on-wafer performances are described by the figure 12. Precisely, the harmonic 2 output power is better than +12 dBm between 55 and 65 GHz output frequency. On the same frequency range, the fundamental output power is lower than –20 dBm, resulting in a fundamental rejection better than 22 dBc.

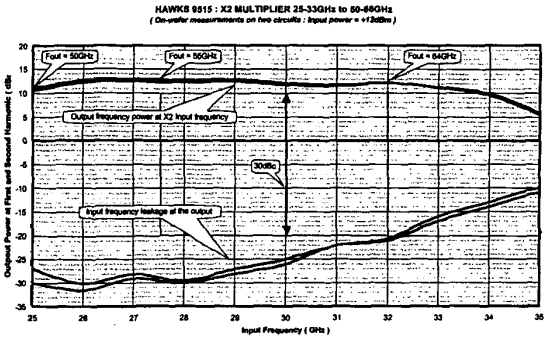

Fig. 12. On-wafer output power measurements of the X2 30→60 GHz.

D. LO frequency multipliers

Generally, the information is transferred from intermediate frequency IF to radio-frequency RF through a mixer, which requires a local oscillator with extremely low phase noise, due to the increasing complexity of the modulation scheme; in that case, people prefer in general to develop oscillators at low frequencies and multiply them by the appropriate factor to meet the LO frequency requirement of their application.

The problem is that each module manufacturer can choose his specific oscillation frequency, depending on his own constraints.

In order to be compliant with most of the 60 GHz applications, UMS has developed two chips to improve the design flexibility of the LO supply chain: a multiplier by 3 and a multiplier by 4. These two MMICs allow to use an input frequency centered respectively on 7.5 and 10 GHz.

The multiplier by 3 (X3) is composed of a tripler stage followed by a 3 stages buffer amplifier. This chip is innovative by the tripler topology based on anti-parallel diodes. This leads to natural rejection of the even harmonics on the output.

Finally, this chip is 2.35 mm² and has a typical biasing point of 125 mA at 3.5 V. Figure 13 exhibits the layout.

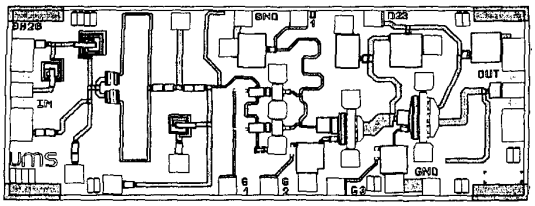

Fig. 13. Layout of the multiplier by 3 (X3).

All the on-wafer measurements are shown on figure 14. With an input power equal to +17 dBm, the harmonic 3 output power is higher than +17 dBm between 7 and 11 GHz, meaning that the conversion gain is better than 0 dB. On the same frequency range, the fundamental and harmonic 2 leakages are below −15 and +5 dBm respectively.

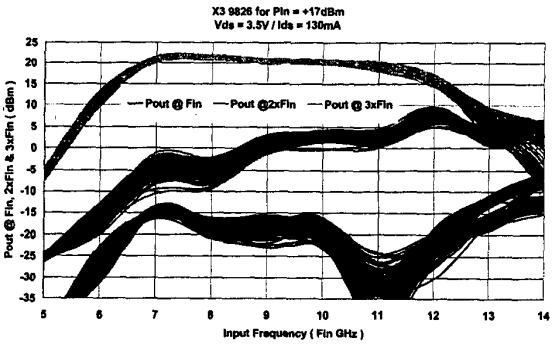

Fig. 14. Multiplier by 3 (X3) output powers @ Fin, 2Fin & 3Fin.

The multiplier by 4 (X4) uses an unbalanced 3 stages topology. The first stage is a multiplier by 2 from 7.5 to 15 GHz, the second stage is also a multiplier by 2 from 15 to 30 GHz and the final stage is a buffer stage covering the frequency range 25-33 GHz.

The on-wafer measurements show a good agreement with simulation. The fourth harmonic output power is between 10 and 13 dBm between 26 and 32 GHz output frequency, the fundamental and second harmonics are lower than 0 dBm, the third shows a positive slope versus the frequency starting at −10 dBm for 26 GHz and finishing at 10 dBm for 32 GHz.

To work properly, this MMIC requires an input power equal to +12 dBm with a DC consumption of 75 mA at Vdd = 3.5 V. The chip size is very compact and equal to 1.8 mm².

IV. Conclusion

This paper describes a full and flexible chipset for V-band applications. It is fully compliant with US, Japanese and European systems, covering the frequency range from 55 to 65 GHz. This chipset is composed of 7 different MMICs, which are intended to be soon available as catalogue products. It is focused on a highly integrated sub-harmonic mixer, leading to 2xLO suppression and image frequency rejection. The other functions are low noise / medium power RF amplifiers (2, 3 and 4 stages), multipliers by 2 (30→60GHz), by 3 (10→30GHz) and by 4 (7.5→30GHz).

All these chips can be protected against humidity and all other external pollution, thanks to a surface passivation layer, avoiding hermeticity requirement at module level.

On-wafer measurements have been performed for all of these MMICs, showing very good results and good agreement with simulation. Measurements of the chipset version with an additional surface passivation layer exhibit minor discrepancies which can be easily compensated by slight modification.

Acknowledgement

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References

[1] O. Vaudescal, B. Lefebvre, A.M. Couturier, R. Sevin, C. Dourlens, P. Quentin, "A highly integrated MMIC chipset for 28 GHz LMDS applications", *Proc. Of 30th European Microwave Conference*, vol. 1, pp. 17-19, Paris, October 2000

[2] O. Vaudescal, D. Kabat, A.M. Couturier, R. Sevin, C. Dourlens, P. Quentin, "A highly integrated MMIC chipset for 40 GHz MVDS applications", *Proc. Of 30th European Microwave Conference*, vol. 1, pp. 216-219, Paris, October 2000

[3] J. Riska, M. Kärkkäinen, P. Kangaslahti, V. Porra, signal generation circuits for 60 GHz wireless broadband system", *Proc. Of 30th European Microwave Conference*, vol. 3, pp. 251-254, Paris, October 2000

[4] K. Hamaguchi et al., "A wireless video home-link using 60 GHz band: concept and performance of the developed system", *Proc. Of 30th European Microwave Conference*, vol. 1, pp. 293-296, Paris, October 2000

[5] M.W. Chapman, S. Raman, "A 60 GHz uniplanar MMIC 4X subharmonic mixer", *IEEE 2001 MTT-S International Microwave Symposium Digest*, vol. 1, pp. 95-98, Phoenix, AZ, May 2001